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EXAMINER	
TRAN, THANH Y	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,495	PARTRIDGE ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-15 and 17-27* is/are rejected.

7)☒ Claim(s) *3,4 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/18/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 9-10, 12, 17-18, 21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Primavera et al (U.S. 2002/0044423).

As to claim 1, Primavera et al discloses in figure 19 a high-density circuit module comprising: a first CSP (first chip 10); a second CSP (second chip 10) disposed above the first CSP (first chip 10) in stacked disposition; a first form standard ("rigid carrier" 70) disposed, in substantial part, above the first CSP (first chip 10); flex circuitry (20) connecting the first and second CSPs (chips 10) and positioned to be, in part, beneath the first CSP (first chip 10) and, in part, above the first form standard ("rigid carrier" 70) and beneath the second CSP (second chip 10), the flex circuitry (20) comprising a first side and a second side and a covercoat ("lid" 80) on each of the first and second sides; at least one metallic bond ("solder mask" 50) attaching the flex circuitry (20) and the first form standard (70) .

As to claim 2, Primavera et al discloses in figure 19 a high-density circuit module further comprising: a second form standard (see "heat sink" 82 as shown in figure 16) disposed, in substantial part, above the second CSP (second chip 10).

As to claims 12 and 23, Primavera et al discloses in figure 19 a high-density circuit module, the flex circuitry (20) is attached to the first form standard ("rigid carrier"70) with at least one metallic bond ("solder mask" 50).

As to claim 9, Primavera et al discloses in figure 19 a high-density circuit module comprising: a first CSP (first chip 10); a second CSP (second chip 10) stacked above the first CSP (first chip 10); a first form standard ("rigid carrier" 70) associated with the first CSP (first chip 10); and a second form standard (see "heat sink" 82 as shown in figure 16) associated with the second CSP (second chip 10); and flex circuitry (20) comprising a first side and a second side and a covercoat (80) on each of the first and second sides.

As to claim 10, Primavera et al discloses in figure 19 a high-density circuit module comprising: flex circuitry (20) connecting the first and second CSPs (chips10).

As to claim 17, Primavera et al discloses in figure 19 a high-density circuit module the flex circuit (20) is attached to the first form standard (70) with adhesive (74) (see paragraph [0059].

As to claim 18, Primavera et al discloses in figure 19 a high-density circuit module and a corresponding method comprising: providing a form standard ("rigid carrier" 70); providing first and second CSPs (chips 10); attaching the form standard (70) to the first CSP (first chip 10); applying a first metallic material (74) to at least one part of the first form standard (70); providing flex circuitry (20) comprising a first side and a second side and a covercoat (80) on each of the first and second sides with an area; disposing the flex circuitry (20) adjacent to the first form standard (70) to create an area of contact; and selectively applying heat to the area of contact (it is capable of creating heat to the area of contact of 20 and 70).

As to claim 21, Primavera et al discloses in figure 19 a stacked circuit module comprising: a CSP (first chip 10); a form standard ("rigid carrier" 70) attached to the CSP (first chip 10); and flex circuitry (20) attached to the form standard (70) and comprising a first side and a second side and a covercoat (80) on each of the first and second sides.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-8, 13-15, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al (U.S. 2002/0044423) in view of Komota (U.S. 2003/0016710).

As to claims 5, 20 and 24, Primavera et al does not disclose the metallic bond comprises at least two metals or tin and gold; the first metallic material is comprised of tin. Komota discloses a metallic bond (adhesive) comprises at least two metals (tin and gold); the first metallic material is comprised of tin (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Primavera et al by using a metallic bond (adhesive) comprises at least two metals (tin and gold) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

As to claim 6, Primavera et al does not disclose a metallic bond is created by combining a first metallic material applied to the first form standard and a second metallic material from

which the flex circuitry is comprised. Komota discloses a metallic bond (adhesive) comprises tin and gold materials (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Primavera et al by using a metallic bond (adhesive) comprises tin (first metallic material) and gold (second metallic material) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

Further, the limitation of "metallic bond is created *by combining a first metallic material applied to the first form standard and a second metallic material from which the flex circuitry is comprised*" is a process limitation in a product claim which does not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA "thin film" 1965).

As to claims 7, 8, and 15, Primavera et al does not disclose the combining of the first metallic material and the second metallic material is achieved through a selected application of heat. Komota discloses a metallic bond (adhesive) comprises tin (first material) and gold (second material) is achieved through a selected application of heat and is achieved with localized friction heating (see paragraph [0058]) (it should be noted that: when a metallic bond (adhesive) is heated it is inherently achieved through a selected application of heat and is achieved with localized friction heating). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Primavera et al by using a metallic bond (adhesive) comprises tin (first metallic material) and gold (second metallic material) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

Further, the limitations of "the combining of the first metallic material and the second metallic material is achieved through a selected application of heat" in claim 7, and "the selected application of heat is achieved with localized friction heating" in claim 8, "the metallic bond *is realized by selective application of heat*" in claim 15 are process limitations in product claims which do not otherwise patentably distinguish over prior art, cannot impart patentability to the product. In re Stephens 145 USPQ 656 (CCPA "thin film" 1965).

As to claims 13 and 14, Primavera et al does not disclose the metallic bond comprises a first metallic material and a second metallic material. Komota discloses a metallic bond (adhesive) comprises a first metallic material (tin) and a second metallic material (gold) (see paragraph [0058]). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the module of Primavera et al by using a metallic bond (adhesive) comprises a first metallic material (tin) and a second metallic material (gold) as taught by Komota for providing a reliable bond formation because known tin and gold materials have high thermal melting bond.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al (U.S. 2002/0044423) in view of Chiang (U.S. 6,803,651).

As to claim 19, Primavera et al does not teach step of using vibration to perform the step of selectively applying heat to the area of contact. Chiang teaches the method of using vibration to perform the step of selectively applying heat to the area of contact (see col. 13, lines 7-10). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and the corresponding method of Primavera et al by

using vibration method for performing heat as taught by Chiang for providing a good bonding connection which is easy to be deformed by vibration (see col. 13, lines 7-10 in Chiang).

6. Claims 26-27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al (U.S. 2002/0044423) in view of Nicewarner, Jr. et al (U.S. 5,776,797).

As to claim 26, Primavera et al discloses in figure 19 a high-density circuit module comprising: a first CSP (first chip 10); a second CSP (second chip 10) disposed above the first CSP (first chip 10) in stacked disposition; a first form standard ("rigid carrier" 70) disposed, in substantial part, above the first CSP (first chip 10); flex circuitry (20) connecting the first and second CSPs (chips 10) and positioned to be, in part, beneath the first CSP (first chip 10) and, in part, above the first form standard (70) and beneath the second CSP (second chip 10), and at least one metallic bond ("solder mask" 50) attaching the flex circuitry (20) and the first form standard (70).

Primavera et al does not disclose the flex circuitry comprising at least two conductive layers.

Nicewarner discloses in figure 3, a flexible substrate 12 comprising at least two conductive layers ("metallized layers" 40 and 42). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and the corresponding method of Primavera et al by having a flex circuitry comprising at least two conductive layers as taught by Nicewarner for forming the inner and outer conductive surfaces for the electrical interconnection between the stacked chips.

As to claim 27, Primavera et al discloses in figure 19 a unit for use in a stacked circuit

module comprising: a CSP (first chip 10); a form standard ("rigid carrier" 70) attached to the CSP (first chip 10); and flex circuitry (20) attached to the form standard (70).

Primavera et al does not disclose a flex circuitry comprising at least two conductive layers.

Nicewarner discloses in figure 3, a flexible substrate 12 comprising at least two conductive layers ("metallized layers" 40 and 42). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and the corresponding method of Primavera et al by having a flex circuitry comprising at least two conductive layers as taught by Nicewarner for forming the inner and outer conductive surfaces for the electrical interconnection between the stacked chips.

7. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Primavera et al (U.S. 2002/0044423) in view of Mukerji et al (U.S. 6,300,679).

As to claims 11 and 22, Primavera et al does not disclose the flex circuitry is comprised of first and second flex circuits.

Mukerji et al discloses in figure 8 a flex circuitry is comprised of first and second flex circuits (810). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus and the corresponding method of Primavera et al by having a flex circuitry is comprised of first and second flex circuits as taught by Mukerji et al for improving the reliability of component/(semiconductor device) by isolating the chip from external stresses.

Allowable Subject Matter

8. Claims 3-4, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments with respect to claims 1-2, 5-15, and 17-27 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9"thin film" 197 (toll-free).

TYT

Kiesha L. Rose
Primary Examiner
Aug. 20, 2007